REMARKS

This is in response to the Office Action dated October 20, 2005. Claims 1-16 are pending. However, claims 8-14 have been withdrawn from consideration.

Claim 1 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Sozansky in view of Papathomas. This Section 103(a) rejection is respectfully traversed for at least the following reasons.

Claim 1 requires that the "solder resist is provided over part of the interconnection pattern but leaves the interconnection pattern exposed in an area that is to be connected to the semiconductor element via the projecting electrode, and wherein the insulating resin containing the anti-repellant covers at least edge portions of the solder resist, and wherein the solder resist is laterally offset and spaced laterally outwardly from an outer edge of the semiconductor element when viewed from above." This underlined feature of claim 1 is advantageous, for example, in that it allows the resin to spread in a desirable manner in direction B during pressing of the chip thereby allowing any rise of the resin to be limited (e.g., see Fig. 1(d) which illustrates direction D, and pg. 23 of the instant specification). As a result, the insulating resin may desirably form a resin fillet by having enough affinity to the side surfaces of the semiconductor element but weak enough to prevent or reduce contact with the pressure applying tool or heat applying tool. Thus, for example, the semiconductor device can realize improvement as to strength and/or reliability of resin sealing.

Sozansky fails to disclose or suggest the aforesaid underlined feature of claim 1. In particular, Sozansky fails to disclose or suggest a "solder resist [that] is laterally offset and spaced laterally outwardly from an outer edge of the semiconductor element when viewed from above" as required by claim 1. Moreover, one of ordinary skill in the art would never have

modified Sozansky to meet the amended claims because Sozansky's chip is a flip chip where the underfill is injected after the chip has already been mounted so that the problem of rising resin is not an issue (col. 7, lines 1-50). Thus, there is no suggestion or motivation in the cited art for any such modification to Sozansky.

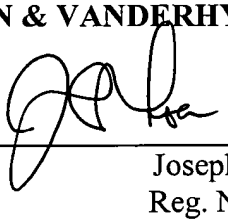
Claim 7 requires that "the solder resist is laterally offset and spaced laterally outwardly from an outer edge of the semiconductor element when viewed from above." Again, the cited art fails to disclose or suggest this feature of claim 7.

Claims 15-16 require that "the solder resist is laterally offset and spaced laterally outwardly from an outer edge of the semiconductor element when viewed from above." Again, the cited art fails to disclose or suggest this feature of claims 15-16.

It is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 

Joseph A. Rhoa
Reg. No. 37,515

JAR:caj
901 North Glebe Road, 11th Floor
Arlington, VA 22203-1808
Telephone: (703) 816-4000
Facsimile: (703) 816-4100